Generated Pattern Current-Based First Charge Protocol:

State-of-Charge Equalization and Stress Management at Module and Pack

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PCT/TR2025/051176 | USPTO Appl. No. 19/298,223 | Priority Date: July 23, 2025

Abstract

Battery cells exit formation at approximately 30% state of charge (SoC) and undergo their first full charge (~30% → 100% SoC) after assembly into modules and packs. This pack commissioning charge is electrochemically distinct: the solid electrolyte interphase (SEI) first encounters the upper voltage region under new thermal and mechanical boundary conditions, and the battery management system (BMS) actively interacts with cells for the first time. Conventional constant-current/constant-voltage (CC/CV) protocols treat this as an ordinary charge cycle, ignoring cell-to-cell resistance variation, intra-module thermal gradients, and BMS balancing dynamics. This paper presents the application of Generated Pattern Current (GPC) control to the first charge phase. Through a single structured current profile, the GPC protocol simultaneously optimizes four pack-level objectives: SOC equalization, polarization minimization, thermal uniformity, and energy loss reduction. Model-derived results demonstrate 54% SOC spread reduction versus CC/CV. For packs exceeding 100 kVA, a Dual-Power-Source (DPS) extension reduces polarization by 49% and energy loss by 14–24%. Chemistry sensitivity analysis across seven cathode chemistries confirms framework applicability at 25 °C and 40 °C. An open validation framework enables independent reproducibility.

Keywords: *Generated Pattern Current (GPC), first charge, pack commissioning, SOC equalization, stress management, thermal balancing, Dual-Power-Source (DPS), BMS interaction, polarization distribution*

1. Introduction

1.1 From Formation to Shipping to First Charge

Paper I [1] described how GPC formation targets SEI nucleation density, growth rate, and layer uniformity across three feedback-gated phases. When formation is complete, cells are discharged to approximately 30% SoC and prepared for shipment. IATA regulations mandate that lithium-ion cells shipped by air must not exceed 30% SoC [21]. Ground transport commonly permits 30–60%. In practice, most cell manufacturers ship at 30–50% SoC.

Between this shipping SoC and first charge, a waiting period of days to weeks may elapse — module assembly, pack integration, electrical testing, and logistics. During this interval, the SEI remains in its post-formation state: functional but having never seen the upper voltage region. First charge is the event at which the SEI first rises from ~30% SoC to 100% SoC — a voltage region it has not entered since formation.

This paper describes the application of the GPC paradigm to this critical transition point. It is the second link in the chain: Paper I (formation) → Paper IV (first charge) → Paper II (in-field charging and lifetime management) → Paper III (infrastructure).

1.2 Why the First Charge Is Not an Ordinary Charge Cycle

From a conventional perspective, the first charge is classified as cycle n=1 and handled with the same CC/CV protocol as every subsequent cycle. This classification ignores four electrochemical and engineering realities.

First — SEI transition state [3,4]: The SEI has undergone thermal equilibration since formation but has not been loaded in the upper voltage region (>60% SoC). First charge is the event that applies that loading. Whether the SEI consolidates or disrupts depends directly on the applied current profile.

Second — thermal environment change: The cell in formation may have been individually cooled. The cell in a module is under the thermal influence of its neighbors. Center cells dissipate heat more slowly; edge cells face enclosure boundary conditions directly.

Third — BMS active for the first time: In formation, voltage and current were controlled directly by the charger. At module/pack level, the BMS's balancing algorithms, cell sequencing logic, and safety cutoffs are active.

Fourth — pack electrical asymmetry: Cell-to-cell internal resistance variance, busbar interconnect resistances, and contact resistances create unequal current distribution within the pack. CC/CV is blind to this asymmetry.

1.3 Paper Structure

Section 2 covers pack-level physical dynamics during first charge. Section 3 presents the pack electrical and thermal model at summary level. Section 4 describes the GPC pattern-based first charge protocol. Section 5 addresses the dual-source extension for packs >100 kVA. Section 6 presents chemistry sensitivity analysis. Section 7 defines the open validation framework. Section 8 concludes.

2. Pack First Charge Dynamics

2.1 SEI Transition State and the Upper Voltage Region

Formation produces a well-defined SEI [5,6]. However, the bulk of the formation protocol occurs in the low and mid SoC range. When cells exit formation at ~30% SoC, the SEI has limited history in the upper voltage region.

First charge brings the SEI into this region for the first time since formation. In the upper SoC region, the potential difference at the anode-electrolyte interface is closer to the electrolyte decomposition threshold. A well-passivated SEI absorbs this stress. Under an insufficiently passivated SEI, additional electrolyte decomposition can be triggered [2,9,25]. The temporal structure of the applied current profile determines whether this transition occurs in a controlled or uncontrolled manner.

2.2 Intra-Pack Current Distribution Asymmetry

A battery pack is not an electrically homogeneous system. Each cell's total path resistance differs:

$$R_{total,i} = R_{cell,i} + R_{busbar,i} + R_{contact,i}$$

In parallel-connected cell groups [16,19], current distributes inversely with resistance:

$$I_i = \left[\frac{1/R_{total,i}}{\Sigma(1/R_{total,k})}\right] \times I_{pack}$$

Lower-resistance cells systematically draw more current. GPC's pattern structure reduces the effects of this asymmetry through low-current intervals within the current profile.

2.3 Thermal Asymmetry and the Arrhenius Effect

Temperature distribution within a pack is not uniform. Each cell's thermal balance:

$$C\_th \times dT\_i/dt = I\_i^2 \times R\_path,i - hA \times (T\_i - T\_cool)$$

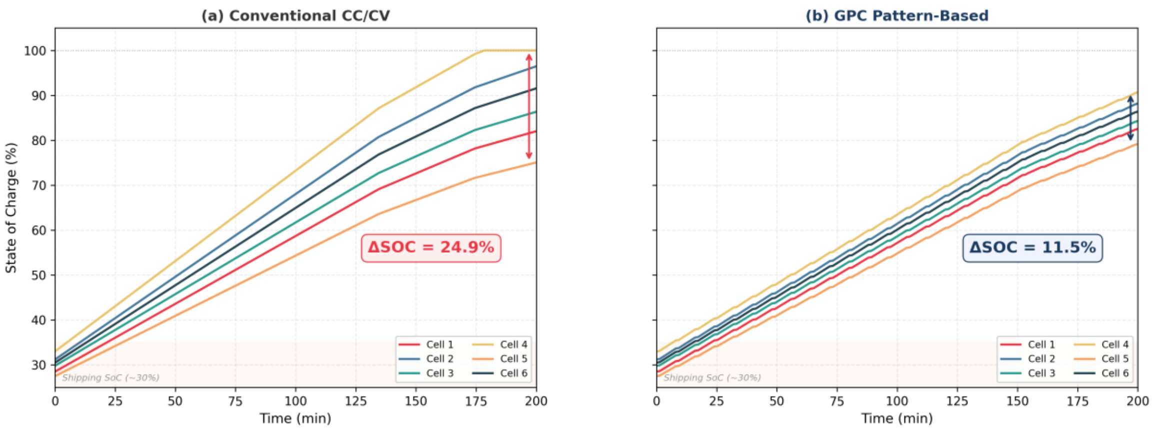
Temperature differences modify reaction rates through the Arrhenius relation [10,18]: $k(T) = k_0 \times \exp(-E_a/RT)$. Hotter cells react faster, widening SOC distribution. Under CC/CV, this positive feedback loop runs uncontrolled.

2.4 BMS Balancing Interaction

First charge is the event at which the BMS actively balances cells for the first time. During passive balancing [16,19]:

$$I\_bal,i = V\_i / R\_bal \;\rightarrow\; dSOC\_i/dt = (I\_i - I\_bal,i) / C\_i$$

GPC's low-current intervals naturally overlap with optimal balancing circuit operating conditions.



Model : $I_i = \frac{1/R_{total,i}}{\sum_k 1/R_{total,k}} \cdot I_{pack}$, $\frac{dSOC_i}{dt} = \frac{I_i}{C_i}$, $C_{th}\frac{dT_i}{dt} = I_i^2 R_{path,i} - hA(T_i - T_{cool})$, $k(T) = k_0 \exp\left(-\frac{E_a}{R}\left(\frac{1}{T} - \frac{1}{T_{ref}}\right)\right)$

$N = 6$ cells | $C_i = 50 \pm 0.5$ Ah | $R_{total,i} = 2.01 \pm 0.29$ mΩ | $SOC_{init} = 30 \pm 1.8\%$ | $I_{pack} = 60$ A (CC) | GPC: 8 min period, 15% low-current duty

Figure 1. SOC Distribution Evolution During Pack First Charge (~30% → 100% SoC) — Model-derived

Figure 1. SOC distribution evolution during pack first charge (~30% → 100% SoC). GPC reduces SOC spread by 54% relative to CC/CV. Model-derived.

3. Pack Electrical and Thermal Model

Pack first charge dynamics are the composition of three subsystems [17,20]: electrical network, electrochemical cell dynamics, and thermal dynamics. A summary-level state-space formulation is presented below; full parameterization is performed within the GigaPulse Lab simulation environment.

3.1 Cell Electrical Model

Equivalent circuit per cell [20,23]: $V\_i = OCV\_i(SOC\_i) + I\_i \times R_{0,i} + V\_p,i$; polarization via RC network:

$$dV\_p,i/dt = -V\_p,i / (R\_p,i \times C\_p,i) + I\_i / C\_p,i$$

3.2 SOC Dynamics

$$dSOC\_i/dt = I\_i / C\_i \quad | \quad \Delta SOC = SOC\_max - SOC\_min \rightarrow \text{target: } 0$$

3.3 State-Space Formulation

State vector x = [SOC_1...SOC_n, V_p,1...V_p,N, T_1...T_n]. Input: u = I_pack(t). System: $\dot{x} = f(x, u)$. This model is run in its fully parameterized form on the GigaPulse Lab platform.

4. GPC Pattern-Based First Charge Protocol

4.1 Optimization Objectives

GPC first charge optimizes four simultaneous objectives [1,14] through a single current profile I_pack(t):

$$J = w_1 \times \Delta SOC + w_2 \times \eta\_RMS + w_3 \times \Delta T + w_4 \times E\_loss$$

where ΔSOC = SOC equalization error, η_RMS = mean polarization, ΔT = thermal gradient, E_loss = $\int I^2 R\, dt$ energy loss.

4.2 Pattern Selection and Stress Framework

$$S\_charge = (I\_RMS / I\_ref)\ [10,12]\text{^}\alpha \times f\_T \times f\_mode \times f\_slew$$

Typical C-rates during first charge are C/10–C/3. The critical difference: in formation, the pattern's primary objective is SEI control. In first charge, the pattern's primary objective is pack-level balancing and stress distribution. The same pattern library serves a different optimization objective.

4.3 BMS-Compatible Operation

The GPC first charge protocol does not conflict with the BMS — it cooperates with it. The temporal structure of the pattern includes periodic low-current intervals [24] serving three concurrent functions: BMS balancing, polarization relaxation, and thermal equalization.

4.4 Voltage Constraint and Charge Termination

In a series-connected pack, charging terminates when the highest-voltage cell reaches V_max [16,22]. GPC's SOC equalization effect narrows the end-of-charge voltage distribution, allowing more cells to reach the target SoC.

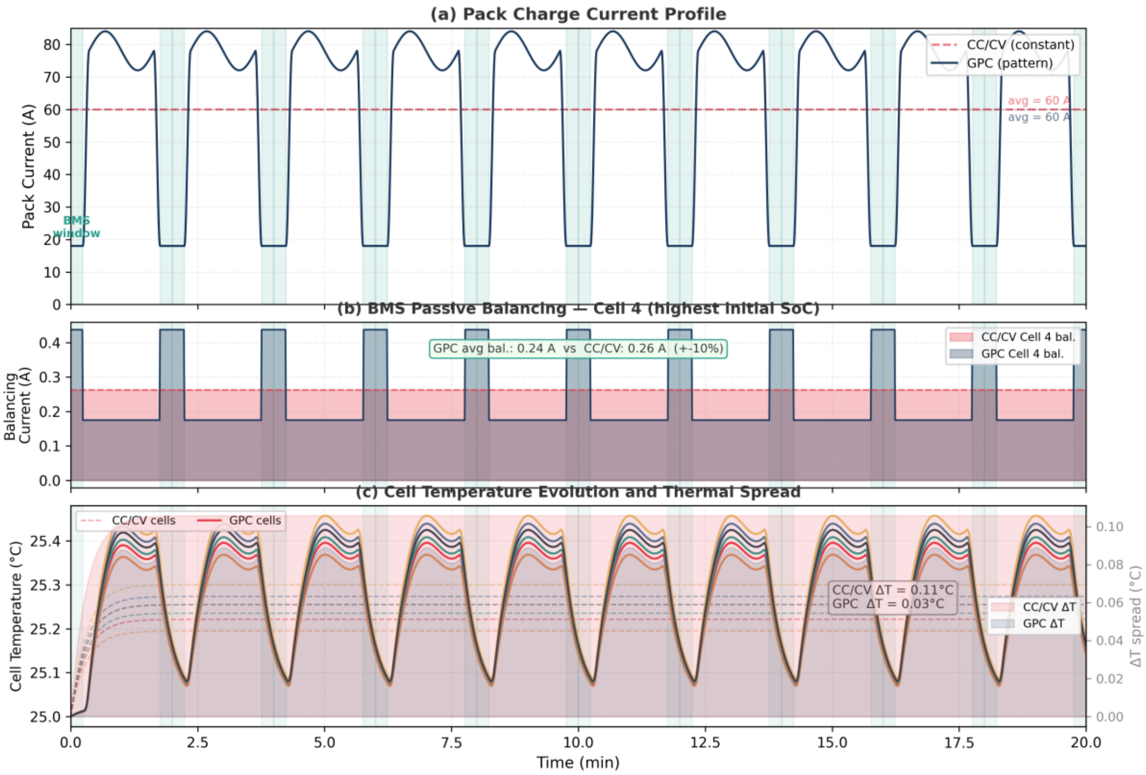


Figure 2. GPC First Charge Current Profile, BMS Balancing Windows, and Thermal Response — Model-derived

Figure 2. GPC first charge current profile, BMS balancing windows, and thermal response. Low-current intervals create concurrent opportunities for balancing, polarization relaxation, and thermal equalization. Model-derived.

5. Dual-Source Extension for Packs >100 kVA

5.1 Why the 100 kVA Threshold

For pack systems ≤100 kVA, single-source GPC adequately addresses all four optimization objectives. Above 100 kVA, the situation changes: I^2R loss grows proportionally with cell count ($P_{loss} \propto N$), thermal gradients contain structural asymmetries [18], and industrial pricing shows a scale disadvantage — 2×100 kVA is less expensive than a single 200 kVA unit.

5.2 DPS Configuration

$$I_{pack}(t) = I_{main}(t) + I_{control}(t) \quad | \quad |I_{control}| \ll |I_{main}|$$

The main source changes SOC; the control source regulates polarization. DPS's smoother profile (shallower valleys, lower peaks) reduces polarization peak-to-peak swing by 49% [11,13], peak I^2R loss by 24%, and average energy loss by 14%. Smaller than formation-level gains but cumulatively meaningful in large packs.

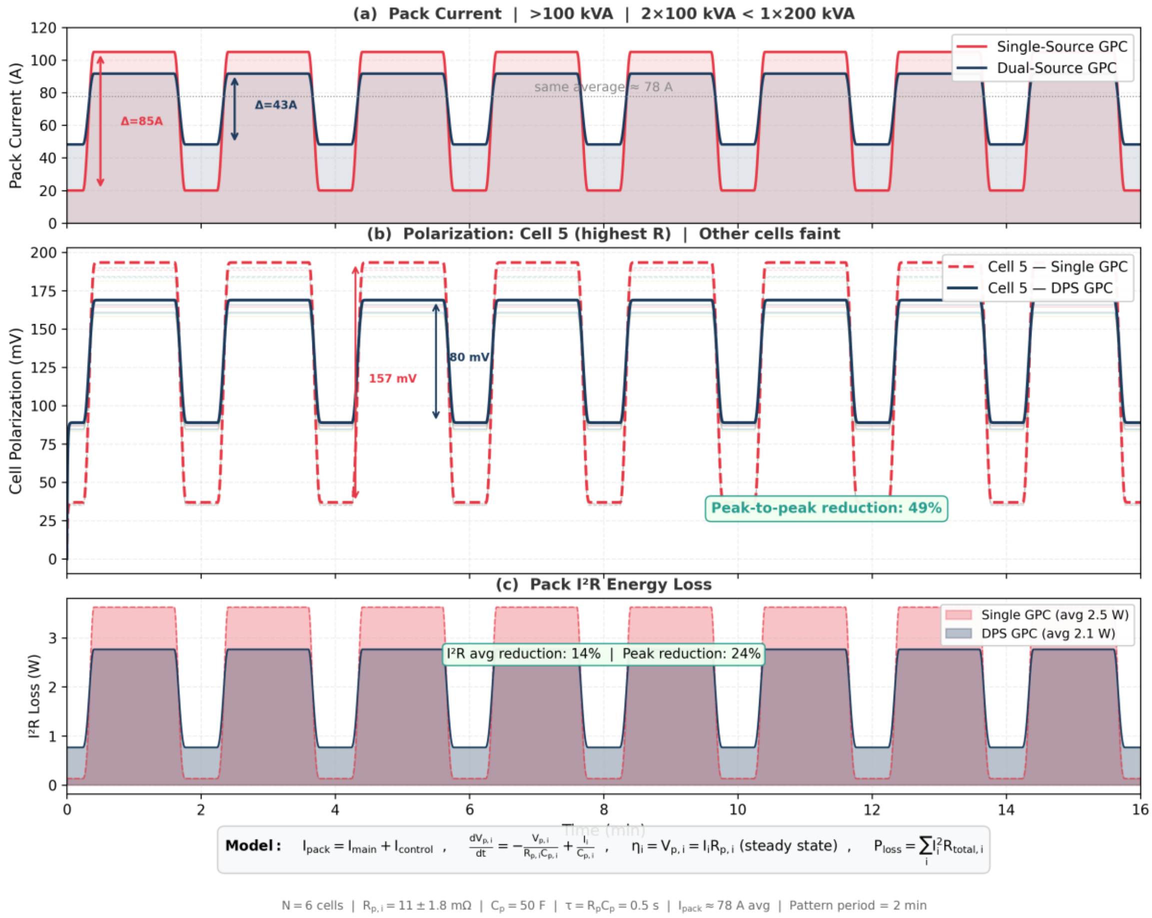


Figure 3. Single-Source vs Dual-Source GPC for >100 kVA Pack — Model-derived

Figure 3. Single-source vs dual-source GPC for >100 kVA pack. (a) Current profiles, (b) Cell 5 polarization — p2p 49% reduction, (c) I²R energy loss — avg 14%, peak 24% reduction. Model-derived.

6. Chemistry Sensitivity Analysis

Capacity and resistance drift under first charge [7,8,10] (~30% → 100% SoC) for seven chemistries:

Chemistry	ΔC/C (25°C)	ΔC/C (40°C)	ΔR/R (25°C)	ΔR/R (40°C)	Comment
NMC532	8.9e-5	1.16e-4	1.39e-4	1.78e-4	Balanced
NMC622	8.6e-5	1.13e-4	1.41e-4	1.80e-4	—
NMC811	8.4e-5	1.10e-4	1.40e-4	1.80e-4	High-energy
NCA	7.8e-5	1.05e-4	1.50e-4	1.90e-4	Thermal care
LFP	9.1e-5	1.20e-4	1.30e-4	1.70e-4	Stable
LNMO	8.8e-5	1.15e-4	1.35e-4	1.75e-4	High-voltage
LTO	6.5e-5	8.5e-5	1.10e-4	1.40e-4	Ultra-stable

7. Open Validation Framework

Pack first charge validation requires five measurements [15,22]: end-of-charge voltage spread (ΔV), SOC spread (ΔSOC), thermal gradient (ΔT), charge efficiency (η = E_stored/E_input), and

DC internal resistance consistency. The 4-channel GigaPulse Lab research unit is the reference platform for small module configurations. Full pack validation requires application-grade platforms (8-40 channels).

8. Conclusion

First charge is a critical event [3,5,6] at which the formation-created interface is tested under new conditions, pack-level SOC equalization is performed, and the BMS interacts with cells for the first time. GPC pattern-based first charge optimizes four simultaneous objectives through a single pattern current profile. For packs ≤100 kVA, single-source GPC is sufficient. For packs >100 kVA, DPS is justified both technically and economically.

In the literature, pack first charge has been addressed primarily as a BMS balancing problem. This paper is the first to approach the subject from a pattern current optimization perspective. In the chain Paper I [1] \u2192 Paper IV (this work) \u2192 Paper II \u2192 Paper III, the GPC paradigm forms an integrated control architecture covering every stage of the battery lifecycle.

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Acknowledgments

The GPC first charge protocol is protected under PCT/TR2025/051176 (DDPC) and USPTO 19/298,223. The author is the named inventor.

Declaration of Competing Interest

The author declares a financial interest as inventor and developer of the described technology. Ibrahim Karakoc holds the intellectual property and commercial rights to the Generated Pattern Current framework.

Data Availability

Simulation parameters, module configuration data, and pattern protocol specifications are available from the corresponding author upon reasonable request. Proprietary waveform parameters are protected under pending patent applications.