Generated Pattern Current for Power Semiconductor Device Conditioning: Interface Trap Stabilization, Quasi-Fermi Level Sweep, and Parametric Drift Control

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PCT/TR2025/051176 | USPTO Appl. No. 19/298,223 | Priority Date: July 23, 2025

Abstract

Power semiconductor devices—Si MOSFET, Si IGBT, SiC MOSFET, and GaN HEMT—require electrical conditioning (burn-in) after manufacturing to achieve parametric stability. Three concurrent physical phenomena govern the conditioning process: interface trap stabilization at the gate oxide–semiconductor interface, oxide charge redistribution in the gate dielectric, and contact resistance stabilization at metal–semiconductor junctions. Conventional DC stress applies a temporally uniform carrier injection profile, fixing the quasi-Fermi level at a single energy position and thereby activating only the subset of interface traps within a narrow energy window near that level. Deep traps, shallow traps, and traps at energies remote from the DC quasi-Fermi level remain unaddressed.

This paper presents the application of the Generated Pattern Current (GPC) paradigm, implemented through the Dynamic Defined Pattern Charging (DDPC) framework, to power semiconductor device conditioning. GPC introduces a time-dependent carrier density n(t) that sweeps the quasi-Fermi level E_Fn(t) across the trap energy spectrum, enabling sequential activation and stabilization of traps at all energy levels. Simultaneously, controlled I^2R_c pulse sequences drive systematic contact and interface micro-annealing, and time-varying oxide field cycling drives Q_ox toward a lower-energy equilibrium. Theoretical analysis predicts 20–40% reduction in conditioning time, improved V_th stability, reduced R_DS(on) drift, and suppression of dynamic R_DS(on) increase in wide-bandgap devices. The GigaPulse Lab platform provides a reference implementation with closed-loop real-time parametric monitoring and adaptive pattern execution.

Keywords: Generated Pattern Current (GPC); Dynamic Defined Pattern Charging (DDPC); power semiconductor conditioning; burn-in; interface trap; quasi-Fermi level sweep; SiC MOSFET; GaN HEMT; threshold voltage stability; dynamic R_DS(on); Shockley-Read-Hall; oxide charge

1. Introduction

1.1 Parametric Instability in Power Semiconductor Devices

Power semiconductor devices do not achieve full parametric stability immediately after manufacturing. Threshold voltage V_th, on-state resistance R_DS(on), gate leakage current, and switching transition parameters all exhibit measurable drift during early device operation [1,2]. This parametric drift originates from three sources in the gate stack and at contact interfaces: the evolution of interface trap occupancy at the gate oxide–semiconductor interface, the

redistribution of charges trapped in the gate oxide bulk and near-interface region, and the microstructural evolution of metal–semiconductor contact junctions under current stress [3].

In silicon-based devices (MOSFET, IGBT), these phenomena are well characterized and are addressed through standard burn-in protocols: elevated-temperature DC stress over defined time and voltage windows [7,8]. In wide-bandgap devices—SiC MOSFETs and GaN HEMTs—the same phenomena occur but are substantially more severe due to the fundamentally different crystal chemistry at the oxide–semiconductor interface. SiC MOSFETs exhibit anomalously high interface trap density D_it at the SiO_2/4H-SiC interface, particularly near the conduction band edge, that reduces channel electron mobility and produces large V_th instabilities under bias stress [4,19,20]. GaN HEMTs exhibit trapping at surface states and buffer defects that causes current collapse: the dynamic R_DS(on) under switching conditions substantially exceeds the static R_DS(on) measured under DC conditions [5,6,9].

1.2 The Limitation of DC Burn-In

Conventional DC burn-in applies a constant gate voltage and drain current, maintaining a fixed carrier density n at the semiconductor surface [25]. The quasi-Fermi level for electrons is determined by n through the Boltzmann relation:

$$E_{Fn} = E_C - kT \cdot \ln(N_C / n)$$

Under constant n, E_Fn is fixed at a single energy position within the bandgap. Shockley–Read–Hall (SRH) trapping kinetics dictate that only traps within approximately kT of the quasi-Fermi level are efficiently filled and stabilized during DC stress [14,15]. Traps at energies substantially above or below E_Fn—deep traps at midgap, shallow traps near the band edges—are not efficiently addressed. The consequence is that DC burn-in converges to a partially stabilized state determined by the DC quasi-Fermi level, with residual parametric drift from the unaddressed trap population [11,12].

This is not a limitation that can be overcome by longer DC stress duration or higher temperature alone. Temperature accelerates trap capture rates uniformly but does not change which traps are addressed—it does not sweep the quasi-Fermi level across the trap energy spectrum. Duration extends the time available for capture at the fixed E_Fn but similarly does not address off-energy traps [3,10]. The fundamental limitation is that a temporally constant carrier density cannot encode the energy information required to address the full trap spectrum.

1.3 GPC as Carrier Injection Temporal Control

Generated Pattern Current (GPC) addresses this limitation by introducing a time-dependent carrier density n(t) through a structured temporal current profile. The core principle, formalized through Jensen's inequality applied to the nonlinear SRH trapping equations, is that the time-averaged response to a structured injection profile differs from the response to the time-averaged injection level:

$$f(\bar{I}) \neq \langle f(n(t)) \rangle$$

where f represents the nonlinear trap occupancy dynamics. When n(t) varies in time, E_Fn(t) sweeps through a range of energies, enabling sequential activation of traps at different energy levels within a

single conditioning protocol. GPC is defined and protected under PCT/TR2025/051176 and USPTO Application No. 19/298,223 (priority date July 23, 2025). The patent scope explicitly covers semiconductor device electrical annealing and carrier injection patterning.

GPC has been applied across multiple domains governed by carrier injection or current injection dynamics: lithium-ion battery SEI formation [22,23], PV cell trap stabilization [24], fuel cell MEA conditioning, and hybrid capacitor activation. In each domain, the governing nonlinear equations respond differently to temporally structured injection compared to the time-averaged constant. Power semiconductor device conditioning presents a particularly direct application because SRH trap dynamics are among the most precisely characterized nonlinear injection-response systems in applied physics [14,15].

1.4 Scope

Section 2 presents the semiconductor device physics governing parametric drift. Section 3 analyzes the three conditioning mechanisms that GPC addresses. Section 4 describes the GPC conditioning protocol design. Section 5 covers SiC- and GaN-specific considerations. Section 6 presents expected conditioning outcomes. Section 7 describes the GigaPulse Lab reference implementation and experimental validation framework. Section 8 discusses implications and generalizations. Section 9 concludes.

2. Power Semiconductor Device Physics

2.1 Sources of Parametric Drift

The threshold voltage of a MOS-gated power device is given by:

$$V_{th} = V_{FB} - \Phi_s - Q_{dep}/C_{ox} - \Delta Q_{ox}/C_{ox} + q \cdot \Delta D_{it} \cdot \varphi_s / C_{ox}$$

where V_{FB} is the flat-band voltage, Φ_s is the surface potential at threshold, Q_{dep} is the depletion charge, C_{ox} is the gate oxide capacitance per unit area, ΔQ_{ox} is the change in oxide trapped charge, and ΔD_{it} is the change in interface trap density at the surface potential φ_s [2,17]. Each of the last two terms represents a drift source that evolves during early device operation. ΔQ_{ox} is driven by hot carrier injection and field-assisted tunneling of charges into oxide traps during current stress. ΔD_{it} evolves as interface trap occupancy changes under carrier injection [11,12].

The on-state resistance $R_{DS(on)}$ depends on channel conductance, which is reduced by interface trap scattering of channel carriers. In SiC MOSFETs, the high D_{it} at the SiO_2/4H-SiC interface directly reduces the effective channel mobility μ_{eff}:

$$\mu_{eff} = \mu_{bulk} / (1 + q \cdot D_{it}/C_{ox})$$

where μ_{bulk} is the bulk semiconductor mobility and the denominator accounts for Coulomb scattering by interface charges [4,20]. Reducing D_{it} through conditioning directly improves μ_{eff} and reduces $R_{DS(on)}$.

2.2 Shockley-Read-Hall Trap Dynamics

The time evolution of trap occupancy N_{occ} at a trap level E_t is governed by the SRH rate equations [14,15]:

$$dN_{occ}/dt = k_c \cdot n(t) \cdot (N_t - N_{occ}) - k_e \cdot N_{occ}$$

where N_t is the total trap density at energy E_t, k_c is the electron capture coefficient, and k_e is the emission coefficient. The emission coefficient depends exponentially on trap energy depth: k_e = σ·v_th·N_C·exp(−(E_C−E_t)/kT), where σ is the capture cross section and v_th is the thermal velocity [3]. For deep traps (E_C−E_t ≫ kT), k_e is exponentially small, and the trap time constant τ_trap = 1/k_e can extend to seconds or longer at room temperature.

The steady-state occupancy under constant carrier density n is N_occ = N_t·k_c·n/(k_c·n + k_e). For traps with E_t far from E_Fn, either k_c·n ≪ k_e (trap above E_Fn: mostly empty) or k_e ≪ k_c·n (trap below E_Fn: mostly filled). Only traps near E_Fn are in a dynamic exchange state and are effectively conditioned by DC stress. This narrow energy window is the fundamental constraint of DC burn-in that GPC overcomes through quasi-Fermi level sweep.

2.3 Gate Oxide Charge Dynamics

Charges trapped in the gate oxide evolve under current stress through competing trapping and detrapping processes [17,18]:

$$dQ_{ox}/dt = k_{trap} \cdot n(t) \cdot (Q_{ox,max} - Q_{ox}) - k_{detrap} \cdot Q_{ox}$$

where Q_ox,max is the saturation trap density, k_trap is the trapping rate coefficient (proportional to injection current density), and k_detrap is the thermal detrapping rate. Under constant n, this equation converges to a steady-state Q_ox = Q_ox,max·k_trap·n/(k_trap·n + k_detrap) that may be far from the minimum-energy oxide charge state. In SiC MOSFETs, near-interface oxide traps (NITs) at energies within 0.1–0.3 eV of the SiC conduction band edge are particularly problematic because their shallow energy makes them highly responsive to gate bias but their large density produces significant V_th shift [19,20].

A time-varying n(t) introduces periodic modulation of the trapping source term, driving the Q_ox toward a different equilibrium than DC stress. The time-averaged Q_ox under GPC injection depends on the temporal structure of n(t) through the nonlinearity of the trapping equation—a direct consequence of Jensen's inequality applied to the trapping dynamics.

2.4 Contact Resistance Evolution

Metal–semiconductor contact resistance at ohmic contacts in power devices evolves during current stress through a thermally activated microstructural process analogous to the graphene contact annealing described for hybrid capacitors [21]. I²R_c heating at contact regions drives local thermal annealing of the metal–semiconductor interface, improving contact morphology, reducing interfacial barrier inhomogeneity, and stabilizing the contact resistance at a lower value. The driving equation is:

$$dR_c/dt = -k_{ann} \cdot I(t)^2 \cdot R_c + k_{rec} \cdot \Delta T_{cool}$$

where k_ann is the annealing rate coefficient and k_rec·ΔT_cool represents partial resistance recovery during thermal relaxation. Under DC stress, continuous I²R heating without controlled relaxation can lead to contact degradation through electromigration accumulation [13]. GPC's pulse structure enables controlled thermal cycling: annealing during high-current

phases, stabilization during low-current phases.

3. Three GPC Conditioning Mechanisms

3.1 Quasi-Fermi Level Sweep for Full Trap Spectrum Coverage

The quasi-Fermi level sweep is the defining mechanism of GPC semiconductor conditioning. When the applied current pattern varies n(t) between n_min and n_max, the quasi-Fermi level oscillates between:

$$E\_Fn,min = E\_C - kT \cdot ln(N\_C / n\_min)$$

$$E\_Fn,max = E\_C - kT \cdot ln(N\_C / n\_max)$$

The energy range ΔE_Fn = E_Fn,max − E_Fn,min = kT · ln(n_max / n_min) covered by the sweep is set by the current modulation ratio n_max/n_min. For a modulation ratio of 10^3 (three decades of current variation), ΔE_Fn ≈ 0.18 eV at 300 K, sufficient to span from shallow near-band-edge traps to mid-gap traps in most power semiconductor materials. For SiC, where the critical trap distribution extends from E_C−0.1 eV to E_C−0.6 eV [19], a modulation ratio of approximately 10^5 would span the full critical energy range.

During the high-current phase (n → n_max, E_Fn → E_Fn,max), deep traps below the raised E_Fn are efficiently captured. During the low-current phase (n → n_min, E_Fn → E_Fn,min), shallow traps near the lowered E_Fn undergo capture-emission cycling that drives them toward equilibrium. The pattern frequency is set to match the trap emission time constant: for a trap at energy E_t, the optimal pattern period is T_pattern ~ 1/k_e(E_t) = exp((E_C−E_t)/kT)/(v_th·σ·N_C). This resonant frequency matching is the trap pumping effect that maximizes conditioning efficiency per cycle [16].

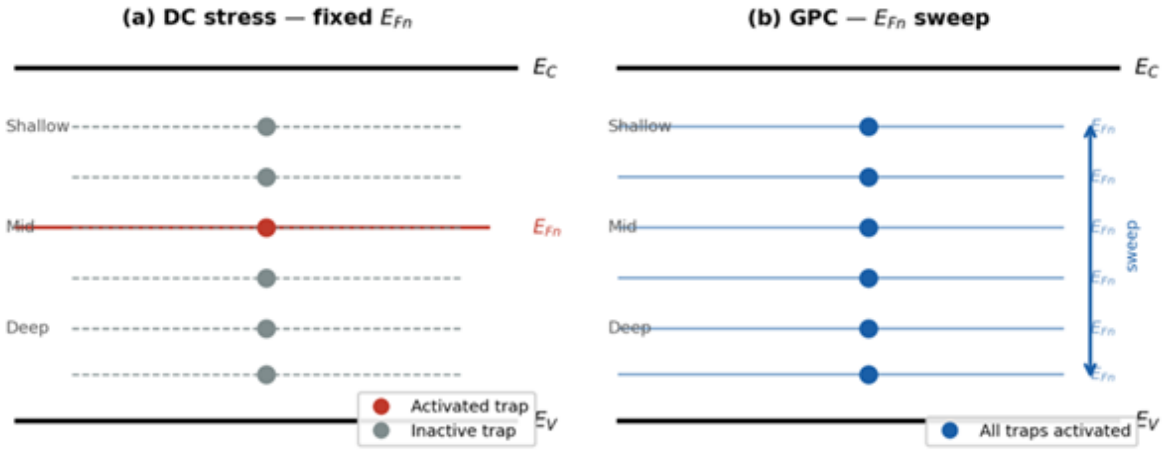

Figure 1. Quasi-Fermi level sweep: (a) DC stress maintains fixed E_Fn, activating only traps within a narrow energy window; (b) GPC oscillation sweeps E_Fn across the full trap energy spectrum, sequentially activating shallow, mid-level, and deep traps.

3.2 Oxide Charge Cycling for Q_ox Stabilization

The oxide charge stabilization mechanism exploits the nonlinearity of the trapping dynamics (Section 2.3). Under DC stress at carrier density n_DC, the oxide charge converges to Q_ox,DC =

$Q_{ox,max} \cdot k_{trap} \cdot n_{DC}/(k_{trap} \cdot n_{DC} + k_{detrap})$. Under GPC with time-varying n(t), the time-averaged trapping rate is $\langle k_{trap} \cdot n(t) \rangle$ but the time-averaged Q_{ox} is determined by the nonlinear steady-state equation evaluated at the time-varying input—not at the time-averaged input. By Jensen's inequality, these differ when the trapping equation is nonlinear, which it is for all practical parameter ranges.

The GPC protocol is designed so that the time-averaged n(t) equals n_{DC} (same mean carrier density as DC stress), while the temporal structure drives Q_{ox} toward a lower-energy configuration. The high-current phases drive the oxide charge toward a high-occupancy state, while the low-current phases allow thermally activated detrapping to reduce Q_{ox}. The net effect of repeated cycling is convergence to a Q_{ox} state that is lower than the DC equilibrium at the same average injection level. This is particularly significant for SiC MOSFETs where Q_{ox}—through its V_{th} shift—is the dominant source of long-term parametric drift [19,20].

3.3 Contact and Interface Micro-Annealing

The micro-annealing mechanism implements controlled I^2R_c thermal cycling at contact and interface regions. High-current GPC pulses produce localized temperature increments $\Delta T_{junction} = I_{pulse}^2 \cdot R_c \cdot R_{th} \cdot t_{pulse}$ at contact junctions, driving thermally activated improvements in contact morphology. The pulse amplitude and duration are set to produce ΔT in the range of 30–60°C above ambient at the junction—sufficient for microstructural annealing without approaching electrolyte or oxide degradation temperatures.

Critically, the electromigration flux J_{EM} is proportional to J^2 [13]. Under DC stress at current density J_{DC}, the electromigration rate is constant and accumulates monotonically. Under GPC with the same time-averaged current density, the high-current phases produce elevated J^2 (accelerated annealing) while the low-current phases reduce J^2 below the DC value, limiting net electromigration accumulation. The asymmetry in the J^2 nonlinearity means that beneficial micro-annealing (proportional to peak J^2) can be enhanced while harmful electromigration accumulation (proportional to time-averaged J^2) is managed—another manifestation of Jensen's inequality applied to a J^2 process.

4. GPC Conditioning Protocol Design

4.1 Pattern Architecture

The GPC semiconductor conditioning protocol integrates the three mechanisms of Section 3 into a composite current profile. The parameter set includes: base conditioning current I_{dc} (determined by device rating and target carrier density), modulation amplitude I_{mod} and frequency $f_{pattern}$ (set by target trap energy range and emission time constants), micro-annealing pulse parameters (I_{pulse}, t_{pulse}, t_{rest}), and total protocol duration determined by convergence criteria.

The frequency selection process begins with DLTS characterization of the target device type to identify the dominant trap levels and their emission time constants

[16]. The pattern frequency f_pattern = 1/T_pattern is set to the emission rate of the dominant deep trap: f_pattern ~ k_e(E_t,deep) = σ·v_th·N_C·exp(−(E_C−E_t,deep)/kT). For SiC MOSFET traps at E_C−0.3 eV, this corresponds to pattern frequencies in the range 10–100 Hz at 300 K. For GaN surface traps with emission time constants of 1–10 ms, pattern frequencies of 100–1000 Hz are appropriate.

4.2 Trap Pumping and Resonant Frequency Matching

The trap pumping effect—enhanced trap stabilization when the pattern frequency matches the trap emission time constant—is a resonant phenomenon that maximizes the number of capture-emission cycles per unit time. At resonance, each pattern period drives the trap through a complete capture-emission cycle, maximally disrupting the DC equilibrium and accelerating convergence to the stable low-energy configuration. Off-resonance patterns still sweep the quasi-Fermi level but do not achieve the resonant enhancement.

For devices with multiple dominant trap species at different energy levels, a multi-frequency GPC pattern can simultaneously target several trap types: I(t) = I_dc + Σ_k I_k·sin(2πf_k·t), where each f_k matches the emission rate of trap species k. This is the semiconductor analog of the frequency decoupling mechanism used for HyCap dual-electrode addressing. The number of frequency components is limited in practice by the bandwidth of the current source and the spectral resolution needed to distinguish trap energy levels.

4.3 GigaPulse Lab Reference Implementation

The GigaPulse Lab platform provides the reference implementation for GPC semiconductor conditioning. The system architecture follows the same topology as other GPC applications: GP Lab connects to the input terminals of a Power Source, which applies the actual current and voltage to the device under test (DUT). GP Lab generates I and V control signals; real-time feedback (measured I, V, T) returns from the Power Source to GP Lab for closed-loop control.

For semiconductor conditioning, GP Lab monitors V_th evolution (from periodic gate sweeps), R_DS(on) evolution (from on-state I-V measurements), and the real-time stress index derived from instantaneous device impedance. The platform's full pattern library—Sinusoidal, SuperPulse, Gaussian, ChemPat, and custom LUT profiles—enables arbitrary carrier injection temporal structures. Application-specific calibration files encode the device-type-specific parameter sets (trap energy targets, emission time constants, current limits) and can be distributed across multiple burn-in stations in a production line. Adaptive termination—replacing fixed-duration burn-in with convergence-criterion-based stopping—reduces mean conditioning time by eliminating unnecessary stress after parametric stability is achieved.

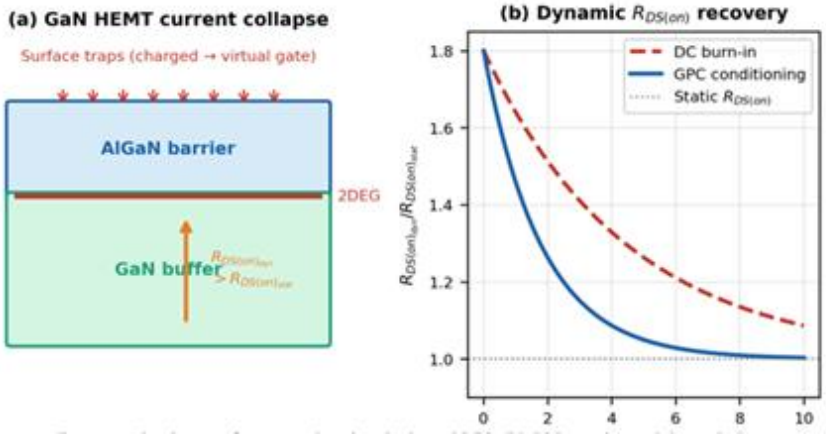

Figure 2. (a) Current collapse mechanism in GaN HEMT: charged surface traps create virtual gate effect, depleting 2DEG and increasing R_DS(on). (b) GPC conditioning accelerates dynamic R_DS(on) recovery compared to DC burn-in through systematic trap stabilization.

5. Wide-Bandgap Semiconductor Specific Considerations

5.1 SiC MOSFET: High D_it and V_th Instability

The SiO_2/4H-SiC interface presents one of the most challenging trap distributions in power semiconductor technology. Interface trap density D_it at the SiO_2/4H-SiC interface is typically 10^{11}–10^{13} $cm^{-2}eV^{-1}$ near the conduction band edge, two to three orders of magnitude higher than at the SiO_2/Si interface [4,20]. This high D_it is attributed to carbon-related defects at the interface and near-interface oxide traps that exchange charge with the SiC conduction band on timescales ranging from microseconds to hours.

The practical consequence is severe V_th instability: threshold voltage drift of 0.5–2.0 V under standard bias stress conditions, compared to <0.1 V for optimized Si MOSFETs [19]. Conventional DC burn-in addresses only traps near the DC quasi-Fermi level and converges slowly because the dominant near-interface traps at E_C−0.1 to E_C−0.3 eV span an energy range that DC injection at typical operating conditions cannot fully cover. GPC quasi-Fermi level sweep, with a modulation ratio tuned to span this energy range, systematically conditions the full near-interface trap distribution within a shorter protocol duration.

5.2 GaN HEMT: Current Collapse and Dynamic R_DS(on)

Current collapse in GaN HEMTs arises from charge trapping at surface states and buffer defects that creates a virtual gate effect: trapped negative charge at the surface depletes the two-dimensional electron gas (2DEG) channel, increasing R_DS(on) transiently after high-voltage switching [5,6,9]. The dynamic R_DS(on) recovery time constant ranges from microseconds to seconds depending on trap energy depth and the specific device structure.

GPC conditioning addresses current collapse through two mechanisms. First, quasi-Fermi level sweep during the conditioning protocol systematically fills and stabilizes surface and buffer traps at different energy levels, reducing the total trappable charge density. Second, pattern frequency matching to the dominant trap

emission time constant drives repeated trap cycling that accelerates convergence to the lowest-energy trap configuration. The result is a reduction in the ratio R_DS(on),dyn / R_DS(on),stat after GPC conditioning compared to DC burn-in at

equivalent duration.

The trap pumping mechanism is particularly effective for GaN because the dominant surface traps have well-defined energy levels and emission time constants accessible to DLTS characterization [16]. Pattern frequencies of 100–1000 Hz, achievable on standard current sources, match the emission time constants of the dominant GaN surface traps.

Sections 2 and 3. The GPC efficiency factor for semiconductor conditioning is defined as:

$$\Psi_{GP,SC} = t_{cond,ref} / t_{cond,GP}$$

where t_cond,ref is the time required under DC burn-in to reach the parametric stability specification and t_cond,GP is the corresponding time under GPC conditioning at equal average carrier density. Based on the trap kinetics analysis, the expected efficiency factor falls in the range Ψ_GP,SC = 1.2–2.0, corresponding to 20–40% reduction in conditioning time. The dominant contribution comes from quasi-Fermi level sweep addressing the full trap energy spectrum; micro-annealing and oxide charge cycling provide additional but smaller contributions.

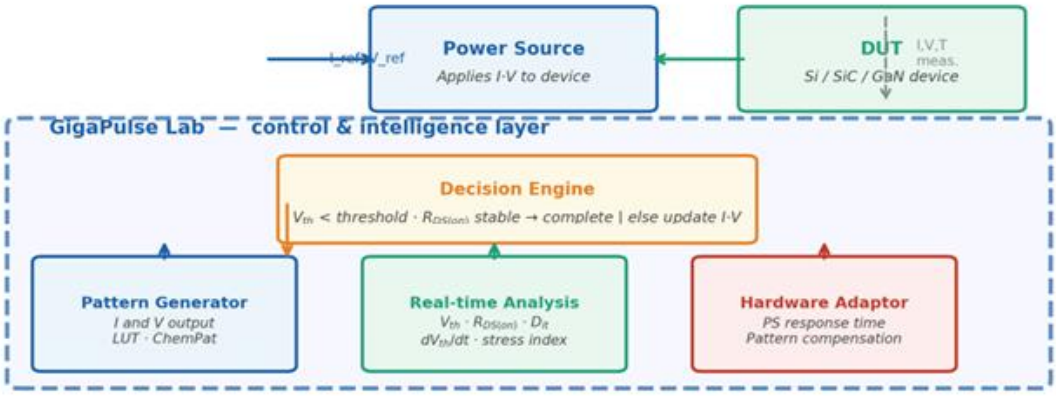

Figure 3. GPC-based power semiconductor conditioning system architecture. GP Lab (control layer) connects to Power Source input terminals and issues I and V pattern signals. Real-time feedback (I, V, T) enables closed-loop V_th and R_DS(on) monitoring and adaptive protocol termination.

6. Expected Conditioning Outcomes

The quantitative predictions for GPC semiconductor conditioning follow from the governing equations analyzed in

Parameter	DC burn-in	GPC conditioning
Conditioning / burn-in time	Reference	20–40% reduction
V_th drift (long-term)	Reference (drift)	Reduced — full trap spectrum conditioned
R_DS(on) drift	Reference	Reduced — lower D_it, better contact
Dynamic R_DS(on) (GaN)	R_dyn ≫ R_static	R_dyn/R_static ratio reduced
Leakage current	Reference	Reduced — oxide charge stabilized
Ψ_GP,SC efficiency factor	1.0 (by definition)	1.2–2.0×
Device yield (lot consistency)	Reference	Improved — narrower parametric spread

Table 1. Predicted conditioning outcomes of GPC protocol compared to DC burn-in baseline.

7. Experimental Validation Framework

7.1 Proposed Protocol

Independent experimental validation requires controlled comparison between DC burn-in and GPC conditioning applied to devices from the same production lot with matched initial parametric distribution. The primary measurement sequence after each conditioning interval includes: V_th from gate voltage sweep at low drain bias (I_D = 1 mA), R_DS(on) from on-state I-V at V_GS = V_GS,rated, off-state leakage I_DSS at V_DS = V_DS,rated, and dynamic R_DS(on) ratio from double-pulse measurement at the rated switching voltage.

DLTS characterization at defined conditioning milestones (0%, 25%, 50%, 75%, 100% of target duration) provides mechanistic attribution: the evolution of trap density at each energy level can be compared between DC and GPC protocols to verify the quasi-Fermi level sweep mechanism. This mechanistic verification distinguishes the validation from a simple performance comparison and provides the physical evidence for the predicted GPC mechanism.

7.2 GigaPulse Lab Integration into Burn-In Station

GPC conditioning can be implemented on any existing burn-in station equipped with a programmable current source. The GigaPulse Lab platform connects to the Power Source input terminals and issues I and V control signals, replacing the static DC voltage/current set-points with dynamically generated pattern signals. No hardware modification of the burn-in station is required beyond the GP Lab control interface connection. The pattern library provides ready-to-use conditioning protocols parameterized for Si, SiC, and GaN device types. Application-specific calibration files are generated from DLTS data for each device family and loaded before conditioning.

For laboratory validation, any programmable current source with bandwidth exceeding the highest pattern frequency (typically 1–10 kHz for semiconductor trap time constants) can implement GPC patterns by waveform upload. Standard semiconductor characterization equipment—parameter analyzers, double-pulse testers, DLTS systems—provides all required

measurement capability without additional instrumentation.

8. Discussion

8.1 GPC Across the Semiconductor Technology Spectrum

The three GPC conditioning mechanisms—quasi-Fermi sweep, oxide charge cycling, and contact micro-annealing—apply across the full range of power semiconductor technologies, though their relative importance varies. In Si MOSFETs and IGBTs, interface trap density is relatively low and D_it conditioning is less critical; the dominant benefit comes from contact micro-annealing and oxide charge stabilization. In SiC MOSFETs, quasi-Fermi sweep addressing the high near-interface trap density is the dominant mechanism. In GaN HEMTs, trap pumping resonant with surface and buffer trap emission times is the primary mechanism. The GPC protocol is parameterized differently for each technology through the device-type calibration file.

8.2 Relationship to Bias Temperature Instability

Bias temperature instability (BTI)—the drift of V_th under sustained gate bias at elevated temperature—is the primary long-term reliability concern for MOS-gated power devices [11,12]. BTI originates from the same oxide charge trapping and interface trap generation mechanisms that GPC conditioning addresses during burn-in. The distinction is temporal: burn-in conditioning occurs at manufacturing on timescales of minutes to hours, while BTI accumulates during device lifetime on timescales of years.

GPC burn-in conditioning reduces the residual trap population that drives BTI by pre-stabilizing traps across the full energy spectrum before device deployment. A device conditioned by GPC has fewer active trapping sites available for BTI-driven drift during field operation. The relationship between GPC conditioning efficiency and long-term BTI reduction is an important topic for experimental validation—devices conditioned by GPC versus DC burn-in should be compared in accelerated BTI lifetime tests to quantify this benefit.

8.3 Generalization to Other Semiconductor Processes

The GPC carrier injection control framework applies beyond device-level burn-in to other semiconductor manufacturing processes where carrier density or current density is a process variable. Dopant activation in implanted layers, where carrier injection accelerates defect annealing through a mechanism formally identical to Section 3.3, represents a particularly promising application discussed briefly in Section 6 of the preliminary analysis. Electrochemical processes in semiconductor fabrication—electrodeposition of contact metals, electrochemical etching—are addressed separately in the GPC series for electrochemical domains.

9. Conclusion

This paper has established the theoretical framework for applying Generated Pattern Current to power semiconductor device conditioning. The fundamental limitation of DC burn-in—that a fixed carrier density cannot address traps across the full

interface trap energy spectrum—is overcome by GPC's time-dependent carrier injection that sweeps the quasi-Fermi level across the trap energy distribution. Simultaneously, controlled I^2R_c pulse sequences drive systematic contact and interface micro-annealing, and oxide charge cycling drives Q_{ox} toward a lower-energy equilibrium.

The governing equations—SRH trap kinetics, oxide charge dynamics, contact resistance evolution—are all nonlinear in the carrier density. Jensen's inequality formally guarantees that the response to temporally structured carrier injection differs from the response to time-averaged constant injection. GPC exploits these nonlinearities through deliberate temporal current design, predicting 20–40% reduction in conditioning time, improved V_{th} stability, reduced $R_{DS(on)}$ drift, and suppressed dynamic $R_{DS(on)}$ in wide-bandgap devices.

The GigaPulse Lab platform provides a reference implementation with closed-loop real-time parametric monitoring and adaptive conditioning termination. Power semiconductor device conditioning is the sixth electrochemical and electrophysical domain in which the GPC paradigm has been analyzed, demonstrating the generality of temporal current structure as an underutilized design variable in applied electronics manufacturing.

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Acknowledgments

The GPC-based semiconductor conditioning protocol is protected under PCT/TR2025/051176 and USPTO Application No. 19/298,223. The author is the named inventor. No external funding was received for the preparation of this manuscript.

Declaration of Competing Interest

Ibrahim Karakoc holds intellectual property and commercial rights related to the Generated Pattern Current (GPC) and Dynamic Defined Pattern Charging (DDPC) technology described in this paper through GigaPulse Energy, Izmir, Turkey.

Data Availability

Data will be made available on request.

Author Biography

Ibrahim Karakoc is the founder of GigaPulse Energy, Izmir, Turkey, where he develops the Generated Pattern Current (GPC) and Dynamic Defined Pattern Charging (DDPC) electrochemical process control technology. His work addresses the application of temporally structured current to a broad range of electrochemical systems including power semiconductor device conditioning, battery management, electrolysis, electrodeposition, and fusion plasma control. He is the named inventor on PCT/TR2025/051176 and USPTO Application No. 19/298,223. He has published a series of papers applying the GPC framework across seventeen electrochemical application domains.